YHM2712A

750mA Linear Charger with Hardware Reset

Features

- 3.4V to 5.5V input range for Efficient Linear Charging
- Programmable Charging Current from 10mA to 750mA by 0.1% external resistor
- Low Dropout Fast Charge, up to 1.5A
- Configurable 4V - 4.525V charging voltage. Preset 4.35V with ±0.5% Accuracy
- Fully Integrated Power Path Switches and No External Blocking Diode Required
- Charging/Discharging Current Monitor Output for Fuel Gauging
- Device Status Output and Access Command Input from STACMD pin
- C/20 Charge Termination
- 2.8V Trickle Charge Threshold
- Built-In Battery Disconnection Function for Shipping Mode with 150nA current consumption
- Built-In Robust Protection Including Input Current Limit, System Short-Circuit Protection, Discharge Current Limit, Battery OVP, Thermal Regulation
- Safety Related Certifications:

  IEC62368-1：2018 CB Certification
- Tiny 0.67mm x 1.02mm 6-pin WLP with 0.35mm pitch

Applications

- Smart Watch/Band
- TWS Earbud
- Bluetooth Portable Device

General Description

YHM2712A is a highly integrated, single-cell Li-ion battery charger with system power path management for space-limited portable applications. The full charger function features Trickle-charge, constant current fast charge and constant voltage regulation, charge termination, and auto recharge.

YHM2712A can deliver up to 750mA charging current, be programmed externally with a single resistor. The charge voltage is default 4.35V and adjustable by Access command. YHM2712A automatically terminates the charge cycle when the charge current drops to 1/20(Default) of the programmed value after the final float voltage is reached. The device can report charging/discharging current for fuel gauging by current monitor output.

Fully Integrated Power Path Switches and no blocking diode is required due to the internal bi-direction MOSFET architecture. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature.

YHM2712A can enter shipping mode by Access command and exit it after input power is present. In shipping mode, battery FET is open and the device only consume 150nA current.

The device status is indicated on STACMD pin output for charging, discharging and charge done. This pin also supports Access command to adjust charging current and charging voltage or enter different mode.

YHM2712A comes in a 6-bump, 0.35mm pitch, 0.67mm x1.02mm wafer-level package (WLP).

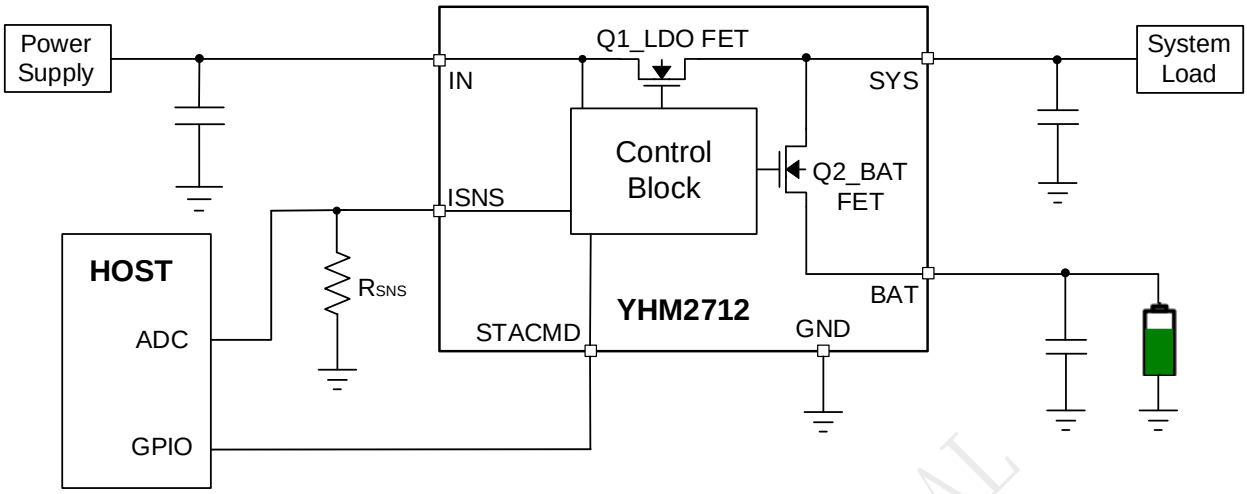


Fig 1. YHM2712A Typical Application

YHM2712A Pin Configurations

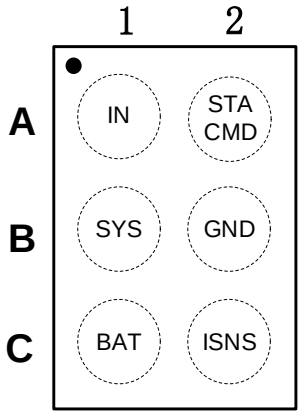


Fig 2. YHM2712A WLP-6 Pin Assignment(Top Through View）

YHM2712A WLP Pin Descriptions

WLP	Name	Description
A1	IN	Input and Power Supply. Bypass this input with a ceramic capacitor to ground.
A2	STACMD	Status Output and Access Command Input. This pin can also be used as push button for hardware reset or exit ship mode, connect push button by 50kohm resistor.
B1	SYS	System power supply. Connect to system load. Place at least 4.7μF ceramic capacitor from SYS to GND, and as close to the IC as possible.
B2	GND	Ground.
C1	BAT	Battery Pin. Place at least 2.2μF ceramic capacitor from BAT to GND, and as close to the IC as possible.
C2	ISNS	Charge Current Program & Monitor Pin. The charge current is programmed by connecting a 0.1% resistor to GND. The voltage on this pin can be used to measure the current between BAT and SYS.

Function Table

STACMD PIN	Status
Low	Charging
High	Other Status except Charging

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Disclaimer: YHMICROS reserves the right to make any change in circuit design, specification or other related things if needed without notice at any time.

Symbol	Parameters		Min.	Max.	Unit
V_{IN}	IN to GND		-0.3	6	V
V_{SYS}	SYS to GND		-0.3	V_{IN} + 0.3	V
V_{OTHER}	Other Pin to GND		-0.3	6	V
I_{IN}	Input Current		0	1500	mA
t_{PD}	Total Power Dissipation at T_A=25°C				mW
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_J	Operating Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
θ_{JA}	Thermal Resistance, Junction-to-Ambient (100mm^2 pad of 1 oz. copper)				°C/W
All Pins	Electrostatic Discharge Capability	Human Body Model, EIA/JESD22-A114	2		KV
		Charged Device Model, JESD22-C101	1		

Note 1. Refer to JEDEC JESD51-7, use a 4-layerboard

2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters	Min.	Max.	Unit
V_{IN}	3.4	5.5	V
I_{IN}	0	800	mA
I_{DISCHG}	0	1500*	mA
I_{CHG}	10	750	mA
V_{OTHER}	0	5.5	V
C_{IN}	0.1		µF
C_{SYS} (at least 3µF of ceramic capacitance with DC bias de-rating)	4.7		µF
C_{BAT}	2.2		µF
Ambient Operating Temperature, T_A	-40	85	°C
Operating Junction Temperature, T_J	-40	150	°C

*1.5A continuous discharge current in 85°C. Peak 2.5A 10ms.

3 Detailed Electrical Characteristics

(V_{IN} = 5V, V_{BAT} = 3.7V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input and Power Path						
Input Voltage Range	V_{IN}		3.4		5.5	V
Input Undervoltage Lockout Threshold	V_{IN_UVLO}	Input Falling		3.2		V
Input Undervoltage Lockout Threshold Hysteresis	$V_{IN\_UVLO\_HYS}$	Input Rising		200		mV
Input vs. Battery Voltage Headroom Threshold	V_{HDRM}	Input Rising vs. Battery		150		mV
Input vs. Battery Voltage Headroom Threshold Hysteresis	V_{HDRM_HYS}			30		mV
Quiescent Supply Current	I_{INQ}	T_A =+25°C, Charge Mode		0.5		mA
		-40°C ≤ T_A ≤ +85°C, Charge Mode			2	
IN to SYS switch on resistance	R_{ON_Q1}	V_{IN} = 5V, I_{SYS} = 100mA		140	250	mΩ
Regulated SYS Output Voltage	V_{SYS}	1.03×V_{REG}		4.48		V
		Accuracy, T_A = +25°C	-5		5	%
Input Current Protection	I_{IN_OCP}			800		mA
Battery Charger						
Battery Quiescent Current	I_{BATQ}	V_{IN} = 5V, Charge Done, I_{SYS} = 0mA		2		μA
		V_{IN} = 0V, V_{BAT} = 4.35V, I_{SYS} = 0mA		20		μA
		Sleep Mode		150	500	nA
		Shipping Mode		150	500	nA
Battery FET on resistance	R_{ON_Q2}	V_{IN} = 0V, V_{BAT} = 3.7V, I_{SYS} = 100mA		50		mΩ
Battery Charge Voltage Regulation	V_{REG}	Default，T_A = +25°C		4.35		V
		Accuracy, T_A = +25°C	-0.5		0.5	%
Fast Charge Current	I_{REG}	R_{SNS} = 25kΩ		20		mA
		R_{SNS} = 10kΩ		50		
		R_{SNS} = 5kΩ		100		
		R_{SNS} = 2kΩ		250		
		R_{SNS} = 1kΩ		500		
		Accuracy, T_A = +25°C, R_{SNS} = 2kΩ	-5		5	%
Regulation Junction Temperature Threshold	T_{J_REG}			120		°C
Trickle-Charge Current	$I_{TRICKLE}$	=0.05×I_{REG}, R_{SNS} = 2kΩ		12.5		mA
Trickle-Charge Threshold Voltage	$V_{BAT\_TRICKLE}$	V_{BAT} Rising	2.7	2.8	2.9	V
Trickle-Charge Threshold Hysteresis				100		mV
Pre-Charge Current	I_{PRE}			4		mA

Pre-Charge Threshold Voltage	V_{BAT_PRE}	V_{BAT} Rising	2	V
Pre-Charge Threshold Hysteresis			100	mV
Termination Current Threshold	I_{TERM}	=0.05×I_{REG}, R_{SNS} = 2kΩ	12.5	mA
Termination Deglitch Time	t_{TERM_DGL}		32	ms
Battery Auto-recharge Voltage Threshold	V_{RECH}	V_{BAT} Falling	120	mV
Battery Auto-recharge Voltage Deglitch Time	t_{RECH_DGL}		120	ms
Over Discharge Current Regulation	I_{DIS_REG}	=10×I_{REG}, R_{SNS} = 2kΩ	2500	mA
Battery Undervoltage Lockout Threshold	V_{BAT_UVLO}	V_{BAT} Falling	2.4	V
Battery Undervoltage Lockout Threshold Hysteresis	$V_{BAT\_UVLO\_HYS}$		200	mV
Battery Overvoltage Protection Threshold	V_{BAT_OVP}	V_{BAT} Rising, higher than V_{REG}	100	mV
Battery Overvoltage Protection Threshold Hysteresis	$V_{BAT\_OVP\_HYS}$		90	mV
System Voltage Threshold for Short Detection	V_{SHORT}		2	V
Shipping Mode				
Enter shipping mode deglitch time	t_{SMEN_DGL}		2	s
THERMAL PROTECTION				
Thermal Shutdown	T_{SHDN}		150	ºC
Thermal Hysteresis	T_{HYST}		20	ºC
LOGIC				
High Voltage of ACMD	V_{IH_ACMD}	1.8V Version	1.17	V
Low Voltage of ACMD	V_{IL_ACMD}		0.3	V
Output High Voltage of STACMD	V_{OH_STA}		1.475	V
Output Low Voltage of STACMD	V_{OL_STA}	I_{SINK}=5mA	0.15	V
ACMD Timing & Specification				
ACMD Line Pull up resistor	R_{PULL}		10	KΩ
Bit Period	t_{BIT}		300	ns
Logic 0	t_{LOG0}		8	t_{BIT}
Logic 1	t_{LOG1}		26	t_{BIT}
Logic Z	t_{LOGZ}		60	t_{BIT}
SWC Rising Time	t_{SRISE}		0.5	t_{BIT}
SWC Falling Time	t_{SFALL}		0.5	t_{BIT}
Two Bit interval	t_{INTV}		1	t_{BIT}

Note 1: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted.

4 Detailed Description

4.1 General Introduction

The YHM2712A is a highly integrated, single-cell Li-ion battery charger with system power path management. The full charger function features Trickle-charge, constant current fast charge and constant voltage regulation, charge termination, and auto recharge. The power path function allows the input source to power the system and charge the battery simultaneously. The device supports private Access command to configure charger without I^2C. The internal bias circuit of the IC is powered from V_{MAX}, which is the higher voltage of either V_{IN} or V_{BAT}. The POR voltage of the device is 1.8V.

4.2 Power Path Management

The YHM2712A employs a pass-through power path structure with the LDO FET(Q1) between IN and SYS, and the battery FET (Q2) between SYS and BAT, to decouple the system from the battery. This allows for separate control between the system and the battery. The LDO output is always regulated to 1.03×VREG. If the V_{IN} is less than target LDO output, the LDO FET is fully turn on to pass through the current. The input current limit threshold is 800mA, when total current for charge and system load is above 800mA, the LDO FET will regulate the current. If the load further increases and V_{SYS} falls below 2V, the device enters hiccup mode. The device also features RCB, when V_{SYS} exceeds V_{IN} by 5mV, the LDO FET will turn off.

4.3 Charge Profile

A charge cycle begins when V_{IN} rises above the UVLO threshold level. If the V_{BAT} is less than 2V, the charger enters Pre-charge mode. In this mode, the YHM2712A supplies 3mA charge current for dead battery. If the V_{BAT} is above 2V and less than 2.8V, the charger enters Trickle-charge mode. In this mode, the YHM2712A supplies approximately 1/20(Default) of the programmed charge current to bring the battery voltage up to a safe level for full current charging. When V_{BAT} rises above 2.8V, the charger enters constant-current mode, where the programmed charge current is supplied to the battery. When V_{BAT} approaches V_{REG}, the YHM2712A enters constant-voltage mode and the charge current begins to decrease. When the charge current drops to 1/20(Default) of the programmed value, the charge cycle ends. When this voltage drops below the recharge threshold, another charge cycle begins and current is once again supplied to the battery.

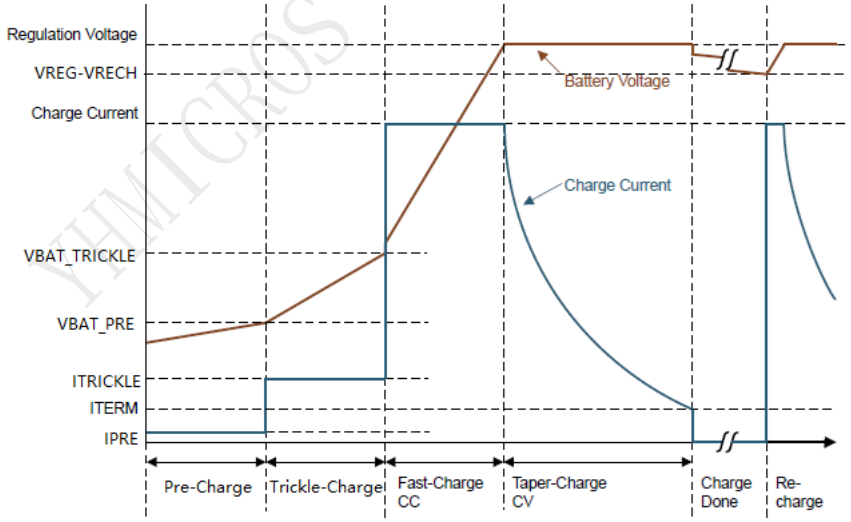


Fig 3. Battery Charge Profile

4.4 Charge Current Programming

The fast charge current is programmed using a single resistor from the ISNS pin to ground. The program resistor and the charge current are calculated using the following equations:

$$R_{SNS} = 500/I_{REG}.$$

The charge current out of the BAT pin can be determined by ISNS pin voltage using the following equation:

$$I_{BAT\_CHG} = V_{ISNS} \times I_{RATIO\_CHG}/R_{SNS}$$

The discharge current into the BAT pin can be determined by ISNS pin voltage using the following equation:

$$I_{BAT\_DCG} = V_{ISNS} \times I_{RATIO\_DIS}/R_{SNS}$$

Connect ISNS pin to an ADC can monitor the charge and discharge current at any time for fuel gauging. When VBAT current is charging mode, I_{RATIO} is 1000. In discharging mode, I_{RATIO} is 5000. I_{RATIO} can be read from ACMD. See below table for detail. In charge done or stop charge mode, the load is supplied by input power, the current monitor does not work.

Mode (02H [7:4])	**VSYS>VBAT** (05H [0])	**ISNS_RATIO** （05H [4]）	**VBAT Current Direction**	**Q2_ratio**
Chg Mode(12)	1	0	Charging	1000
Chg Mode(12)	0	0	Discharging	5000
DisChg Mode(8)	x	0	Discharging	5000

Table 1. Current Ratio

4.5 Low Dropout Fast Charge

YHM2712A supports low dropout fast charge, up to 1.5A charging current. When V_{IN} is above UVLO and below V_{REG}, Q1 will enter bypass mode. Then configure 00H[0]=1 to disable Q1 800mA current limit, 00H[3]=1 to disable headroom voltage and configure 01H[7:5] to choose the actual charging current for fast charge. Configure 03H[5]=1 can make Q2 fully on for directly charging.

4.6 Battery Discharge

When V_{IN} is above UVLO threshold level, system is power by input from LDO FET. When V_{SYS} drop to below V_{BAT} by 5mV, the BAT FET turn on and battery start to supply current to system load. If V_{SYS} rise to V_{BAT} plus 5mV, BAT FET goes back to charge mode. The YHM2712A has an over-discharge current limit in discharge mode. Once the discharge current exceeds the programmable discharge current limit ($10\times I_{REG}$), the battery FET will regulate the current.

4.7 Thermal Regulation and Thermal Shutdown

The YHM2712A will reduce the programmed charge current by half if the die temperature attempts to rise above 120°C. This feature protects the YHM2712A from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the chip. When the junction temperature reaches 150°C, both Q1 and Q2 turn off.

4.8 System Short-Circuit Protection

The YHM2712A features SYS node short-circuit protection (SCP) for both the IN to SYS path and the BAT to SYS path. The system voltage is monitored continuously. When V_{SYS} is lower than 2V consecutively for 60μs, the chip enters FAULT mode and both Q1 and Q2 will be turned off, hiccup 2ms later.

4.9 Shipping Mode

At any point in the charge cycle, the YHM2712A can be put into shipping mode by Access command for 2s. In shipping mode, BAT FET turns off and the device only consume 150nA current from battery. Plug V_{IN} to wake the YHM2712A up from shipping mode.

4.10 Current Test Mode

When V_{IN} exceed 6V for 2ms or set by Access command, the YHM2712A will enter current test mode. In this mode, Q2 turn off and the system current can be measured from input power supply. In test mode, the chip does not have over current protection, recommend add external OVP/OCP device in test cable. Remove V_{IN} to exit the current test mode.

4.11 Sleep Mode

YHM2712A can enter sleep mode by configuration. In sleep mode, battery Iq is only 150nA, the recommended discharge current is below 10mA. Before system wake up for large load, need to configure YHM2712A to exit sleep mode first.

4.12 Hardware Reset

Pull STACMD down to GND for 14.4s, the device will shut down SYS for 200ms and automatically powering it back on. Choose a GPIO to connect to STACMD for communication which is high impedance when MCU is power off.

4.13 Status

The STACMD pin can indicate charging, discharging and charge done status. When it is high, the battery is in discharging or charge done. When it is low, the battery is in charging.

5 Access Command

YHM2712A supports private Access Command(ACMD) from STACMD pin to configure the charger. Access command is a single wire communication protocol developed by YHMICROS. There are two type devices, master and slaver, in this protocol. The master can send control command to slaver and read slaver status. The slaver can only respond master instruction. Only the master can initial communication in Access command. The 7bit slave address of YHM2712A is 04H in normal mode.

5.1 ACMD Physical Layer

The communication line in ACMD is pull high with internal resistor. This line keeps in high voltage level if there is no communication signal. ACMD master or slaver can pull low this line if they need send data on this line. There are three waveforms to indicate three logic statuses (Logic 0, Logic 1 and Logic Z). These waveforms are different from their low pulse width. Please refer to below figure.

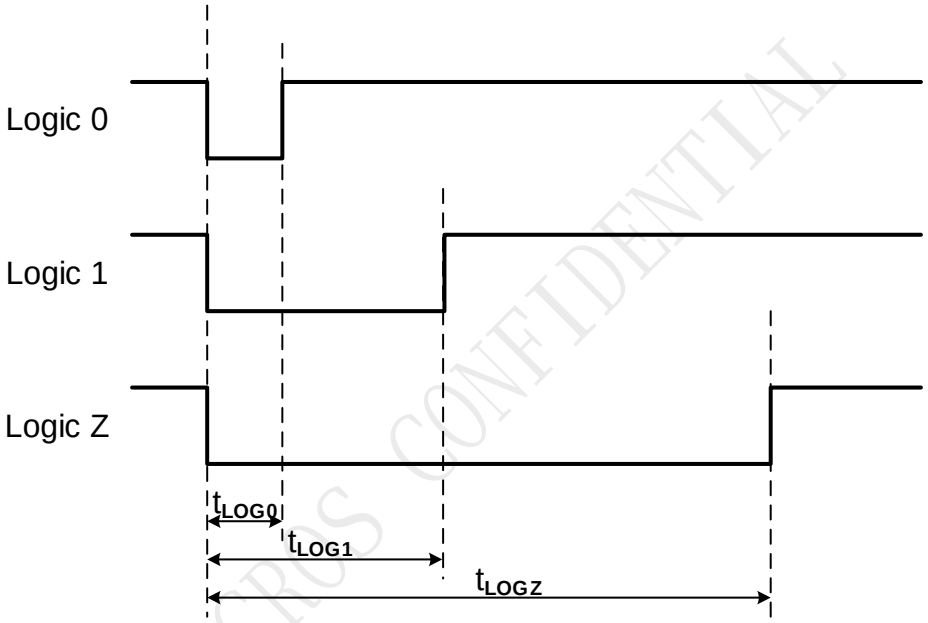


Figure 4. ACMD Logic Bit

Logic 0's low voltage width is 8 t_{BIT}, Logic 1's low voltage width is 26 t_{BIT} and Logic Z's low voltage width is 60 t_{BIT}. Logic 0 and Logic 1 are used to normal data communication. Logic Z is used as START, RE-START and STOP bit in data package. When device received Logic Z, it will reset internal status machine and intermediate variables in ACMD protocol. Please note, because master and slaver can pull down the communication line, the total low voltage period is AND operation for both master TX signal and slave TX. Figure 5 indicates this situation.

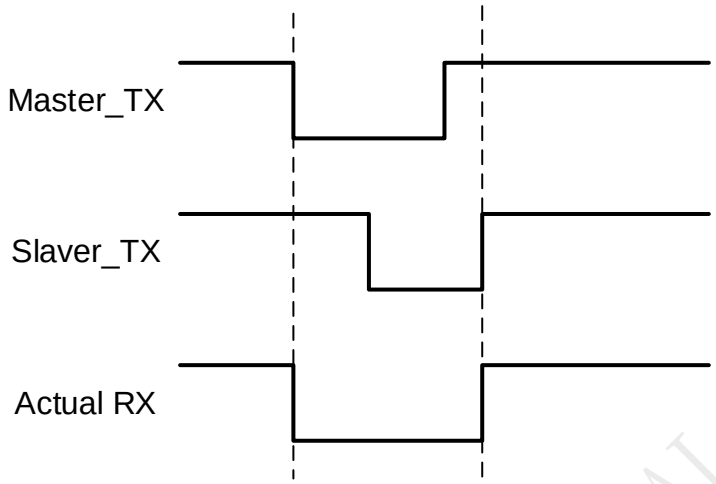


Figure 5. RX Behavior if Master and Slaver Drive Line Together

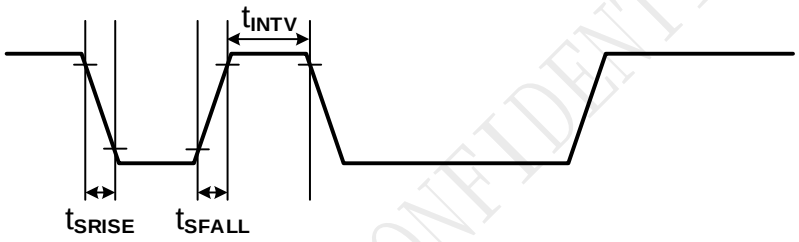


Figure 6. ACMD Bit Timing

5.2 ACMD Protocol Layer

One ACMD data package is formed one START signal, data and STOP signal. Logic Z servers as START, RE-START and STOP signal role. When slaver receive one start signal, it reset status machine and wait for the data from line. It continues to receive data or send back to the master until it receives one STOP bit. Data character is formed with 8 bits data plus 1 bit parity. This parity is sent from the other side in communication. For example, if data is from the master, slave sends this parity as ACK for received one character data and the master check this bit to know the slave received data correct or not. Please note in the last data character, master send NACK to slave. NACK is NOT operation to ACK. Data character is MSB firstly. YHMICROS ACMD write and read operations include two options. One is normal device addressing mode. The other is short device addressing mode. In normal device address mode, the device has 6-bit device address (64 devices) and 8-bit register address (256 registers). It is used for large register address numbers device. In short device addressing mode, the device has 2-bit device address (4 devices) and 4-bit register address (16 registers). This means one ACMD line can support 4 slaver devices at most in short mode. But in this mode, the register number is less than the normal mode.

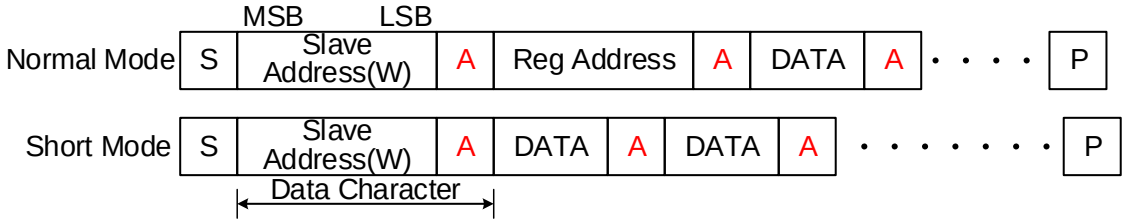


Figure 7. Write Operation in ACMD

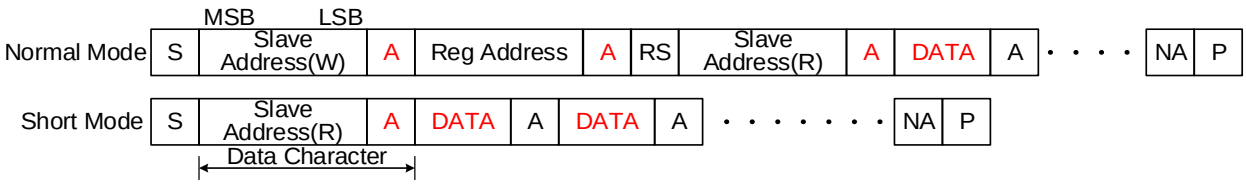


Figure 8 Read Operation in ACMD

In above figure, red bit is sent from slaver and the others is sent from master. The slave address character description is listed below.

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A
Normal	Mode flag. 0: Normal mode. 1: Short mode	Device Address						Write/Read flag. 0: Write 1: Read	ACK from Slaver. Parity of Bit [7:0]
Short		Device Address		Register Address					

Table 2. Slave Address Character

Register Map

Addr	ID	Default	B7	B6	B5	B4	B3	B2	B1	B0
00H	V_CTRL	60H	VREG[3:0]				VHDRM	VTRICKLE	Q1_RCB	Q1_ILIM_DIS
01H	I_CTRL	00H	ICC[2:0]			ITERM	ITRICKLE	IPRE_VBAT	SYS_TRACK	RESERVED
02H	MODE	A0H	MODE[3:0]				M_SET	BAT_OV_DIS	RST_REG	HD_RST
03H	CONFIG	00H	RESERVED	ITERM_DIS	CC_DIS	WD_RST	WD_EN	VRECH	DIS_VIN_ITEST	FT_DEB_TIME
05H	STATUS1		CHG_STATUS[2:0]			ISNS_RATIO	TSD_120	TSD_150	ISNS<ITERM	VSYS>VBAT
06H	STATUS2		FSM MODE[3:0]				VBAT>2	VBAT> VBAT_TRICKLE	VBAT_OV	VBAT_UV
07H	STATUS2		CV_BAR				RESERVED			
08H	ID	A0H	Vendor				Revision			

V_CTRL Register

Address: 00h

Type: Read/Write

Bits	Name	Defaults	Description	Comment
7:4	VREG[3:0]	0 1 1 0	0000: 4.2V；0001: 4.225V； 0010: 4.25V；0011: 4.275V； 0100: 4.3V； 0101: 4.325V； 0110: 4.35V；0111: 4.375V； 1000: 4.4V；1001: 4.425V； 1010: 4.45V；1011: 4.475V； 1100: 4.5V；1101: 4.525V 1110: 4V； 11111: 4.1V；	Battery regulation voltage. Default: 4.35V
3	VHDRM	0	0: 150mV Headroom voltage 1: No Headroom voltage	V_{IN} Vs V_{BAT}
2	VTRICKLE	0	0: 2.8V 1: 3V	Trickle-charge to fast charge threshold. Default 2.8V.
1	Q1_RCB	0	0: V_{SYS} - 5mV > V_{IN} 1: V_{SYS} +5mV > V_{IN}	Input reverse blocking voltage threshold. Default trigger condition is V_{SYS} - 5mV>V_{IN}.
0	Q1_ILIM_DIS	0	0: 800mA 1: Disable Q1 ILIM	Disable Q1 current limit, default is 800mA

***Configure VHDRM=1 and Q1_RCB=1 and CC_DIS=1 to support bypass mode.*

I_CTRL Register

Address: 01h

Type: Read/Write

Bits	Name	Defaults	Description	Comment
7:5	ICC[2:0]	0 0 0	000: 0.5×I_{REG}；001: 0.2×I_{REG}； 010: 0.7×I_{REG}；011: 0.9×I_{REG}； 100: I_{REG}；101: 1.5×I_{REG}； 110: 2×I_{REG}；111: 3×I_{REG}	Fast charge current I_{CC}. Default: I_{CC} = 0.5×I_{REG} (000) I_{REG} is set by R_{SNS}
4	ITERM	0	0: 0.05×I_{REG}	Termination current.

			1: 0.1×I_{REG}	Default: 0.05×I_{REG} I_{REG} is set by R_{SNS}
3	ITRICKLE	0	0: 0.05×I_{REG} 1: 0.1×I_{REG}	Trickle charge current. Default: 0.05×I_{REG} I_{REG} is set by R_{SNS}
2	IPRE	0	0: 4mA 1: 12mA	Pre charge current.
1	SYS_TRACK	0	0: Disable SYS_TRACK，VSYS=1.03*VREG during charging, Q1 limit 800mA 1: Enable SYS_TRACK，VSYS=1.053*VBAT during charging, Q1 limit 275mA	
0	RESERVED			

MODE Register

Address: 02h

Type: Read/Write

Bits	Name	Defaults	Description	Comment
7:4	MODE[3:0]	1010	0000: RESET 0001: SHIPPING 0010: SLEEP 0011: ITEST 0100~0111: RESERVED 1000: DISCHARGE 1001: FAULT 1010: START 1011: SYS_PRE 1100: CHARGE 1101: CHARGE_DONE 1111: STOP_CHARGE	Valid when write M_SET=1 1111: STOP_CHARGE 0011: ITEST 0001: SHIPPING 0010: SLEEP When exit above mode, must exit to correct mode*
3	M_SET	0	0: No Action 1: Set FSM mode as MODE [3:0]	Auto Clear
2	BAT_OV_DIS	0	0: Enable BAT OV 1: Disable BAT OV	
1	RST_REG	0	0: No Action 1: Reset Reg	Auto Clear
0	HD_RST	0	0: No Action 1: POR	Auto Clear

***Check VIN OK before enter stop charge mode.*
**Write MODE[3:0]=1100 if want to exit Stop Charge Mode*
**Write MODE[3:0]=1000 if want to exit Sleep Mode*
**Write MODE[3:0]=1010 if want to exit ITEST Mode or Shipping Mode*

CONFIG Register

Address: 03h

Type: Read/Write

Bits	Name	Defaults	Description	Comment
7	RESERVED			
6	ITERM_DIS	0	0: Termination is enabled 1: Termination is disabled	
5	CC-DIS	0	0: Q2 CC is enabled 1: Q2 CC is disabled	
4	WTD_RST	0	0: Default 1: Reset WD wait timer (Clear to 0 after write)	Auto Clear
3	WD_EN	0	0: Disable 1: Enable watch dog	16s WDI wait time. When timer out, turn off Q1&Q2 for 200ms then enter start up mode
2	VRECH	0	0: 200mV 1: 100mV	Battery Recharge Voltage Threshold
1	DIS_VIN_ITEST	0	0: Enable 1: Disable	0: Enable V_{IN}>6V enter current test mode.
0	FT_DEB_TIME	0	0: 2ms 1: 100ms	Fault hiccup time

STATUS1 Register

Address: 05h

Type: Read Only

Bits	Name	Defaults	Description	Comment
7:5	CHG_STATUS		000: Discharge 001: Pre-Charge 010: Trickle-Charge 011: CC Charge 100: Reserved 101: CV Charge 110: Reserved 111: Charge Done	
4	ISNS_RATIO		0: 5000 1: Reserved	Discharge current sense ratio
3	TSD_120		0: T_J<120°C 1: T_J>120°C	
2	TSD_150		0: T_J<150°C 1: T_J>150°C	
1	ISNS<ITERM		0: I_{SNS}>I_{TERM} 1: I_{SNS}<I_{TERM}	
0	VSYS>VBAT		0: V_{SYS}<V_{BAT} (Discharge) 1: V_{SYS}>V_{BAT} (Charge)	

STATUS2 Register

Address: 06h

Type: Read Only

Bits	Name	Defaults	Description	Comment
7:4	FSM_MODE		0000: RESET 0001: SHIPPING 0010: SLEEP 0011: ITEST 0100~0111: RESERVED 1000: DISCHARGE 1001: FAULT 1010: START 1011: SYS_PRE 1100: CHARGE 1101: CHARGE_DONE 1111: STOP_CHARGE	
3	VBAT>2		0: V_{BAT}<2V 1: V_{BAT}>2V	
2	VBAT> VBAT_TRICKLE		0: V_{BAT}< $V_{BAT\_TRICKLE}$ 1: V_{BAT}> $V_{BAT\_TRICKLE}$	
1	VBAT_OV		0: V_{BAT}< V_{REG}+100mV 1: V_{BAT}> V_{REG}+100mV	
0	VBAT_UV		0: V_{BAT}>2.4V 1: V_{BAT}<2.4V	

STATUS3 Register

Address: 07h

Type: Read Only

Bits	Name	Defaults	Description	Comment
7	CV_BAR		0: In CV 1: Not in CV	CV need meet below condition: 05H[7:5]=101 and 07H[7]=0
6:0	RESERVED			

ID Register

Address: 08h

Type: Read Only

Bits	Name	Defaults	Description	Comment
7:4	Vendor	1010		
3:0	Version	0000		

6 Control Flow Chat

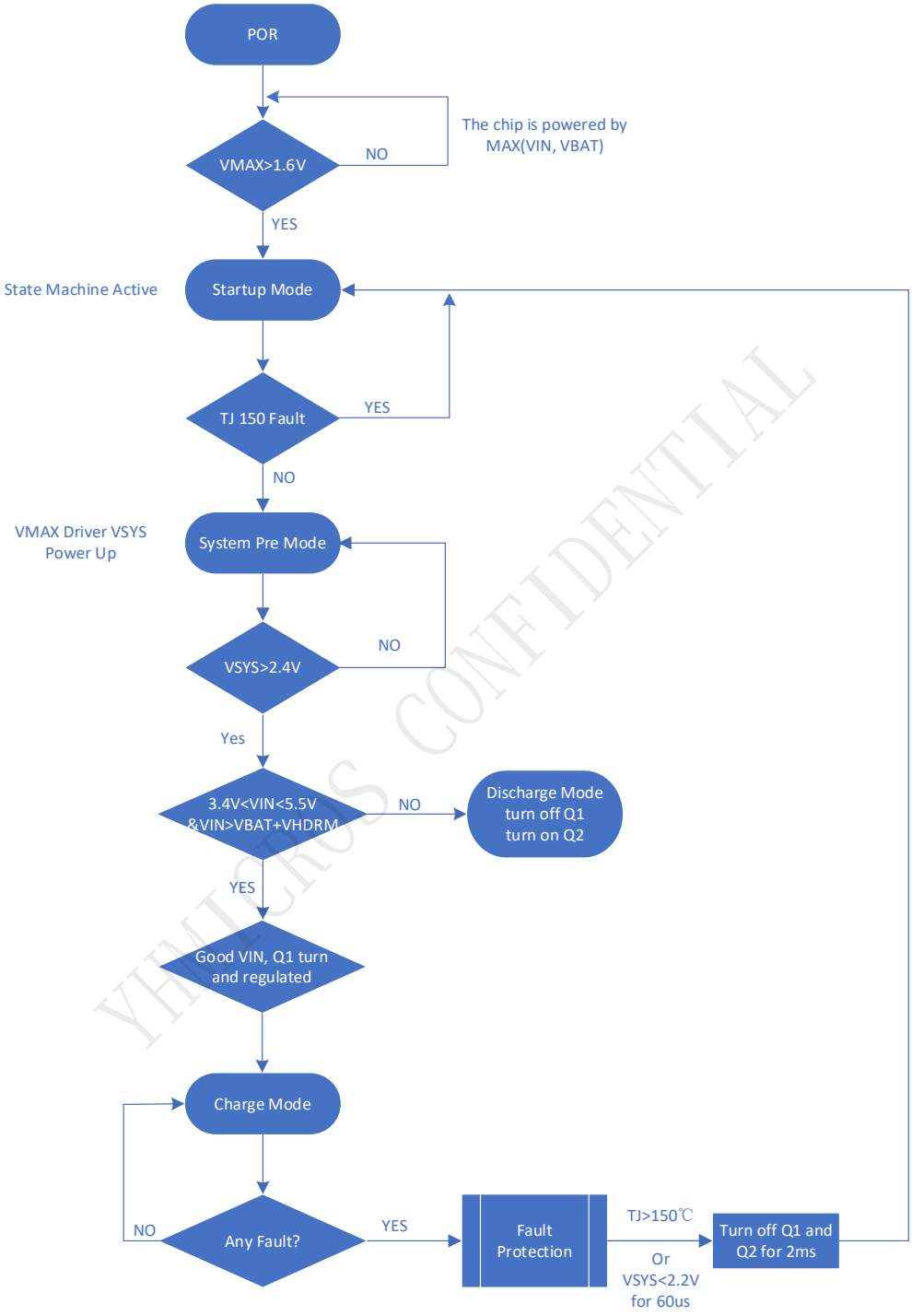


Fig 9. Startup Flow Chat

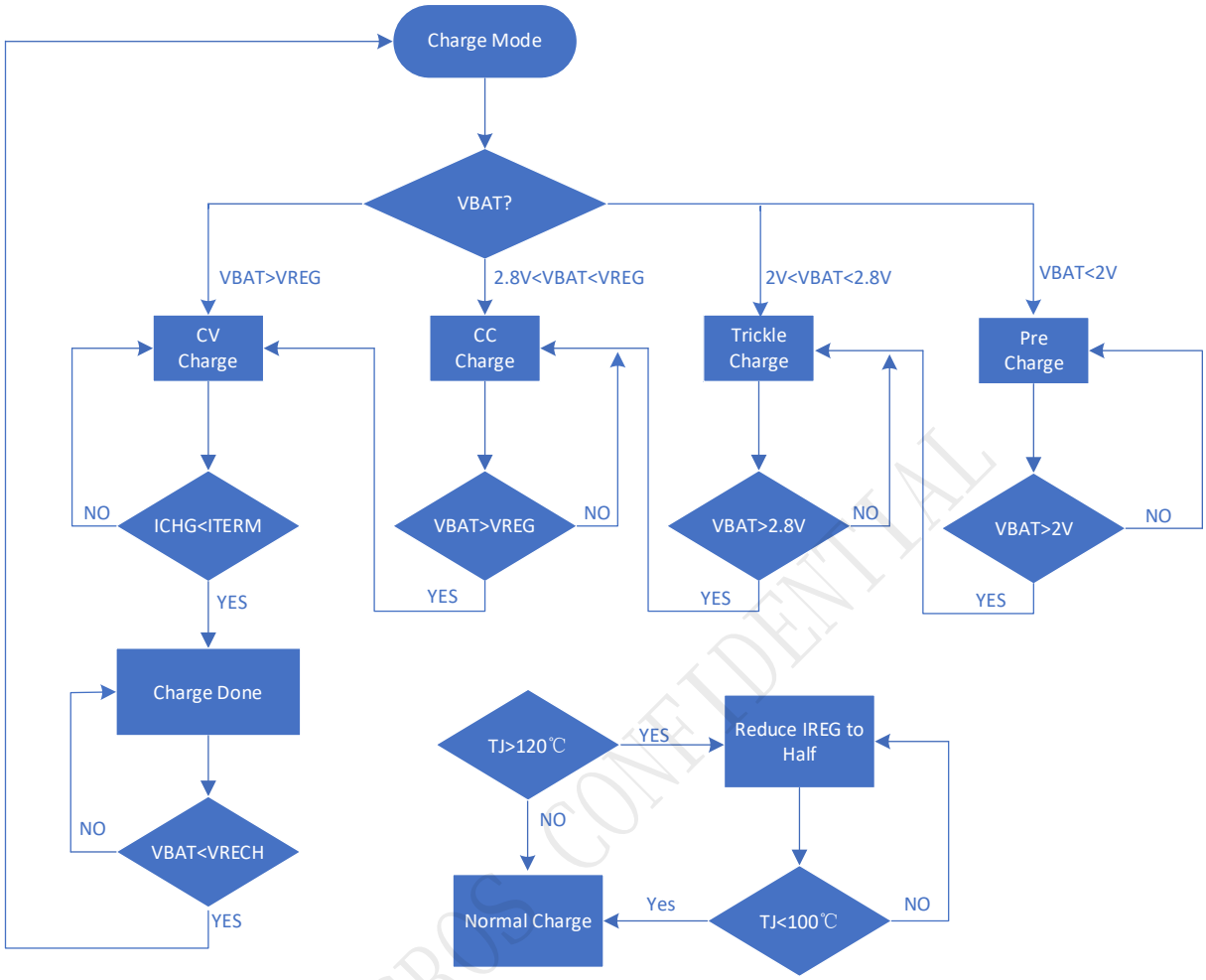


Fig 10. Charging Flow Chat

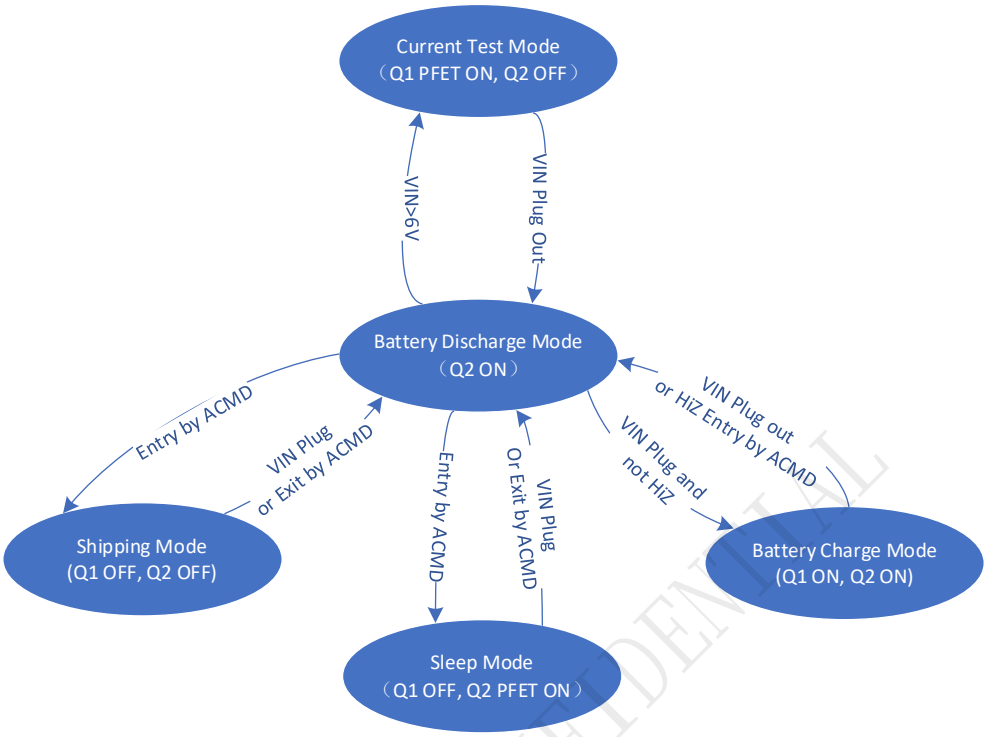
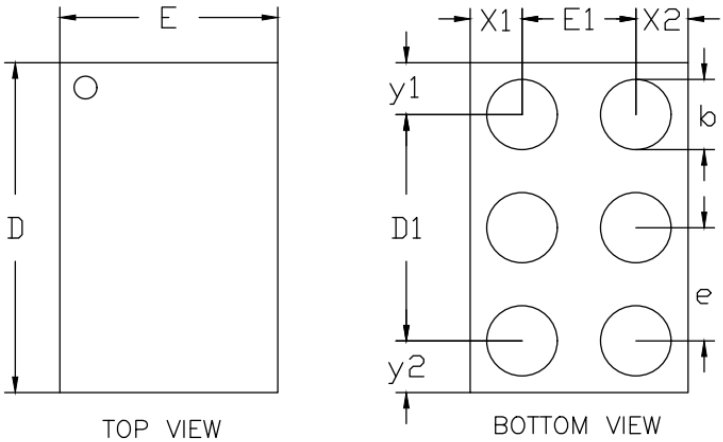
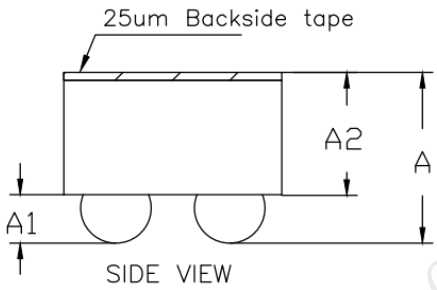


Fig 11. State Machine Conversion

Package Dimensions

WLCSP-6 0.67x1.02





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.483	0.528	0.573
A1	0.130	0.150	0.170
A2	0.353	0.378	0.403
D	1.000	1.020	1.040
D1		0.700BSC	
E	0.650	0.670	0.690
E1		0.350BSC	
b	0.200	0.220	0.240
e		0.350BSC	
x1		0.160 REF	
x2		0.160 REF	
y1		0.160 REF	
y2		0.160 REF	

Ordering Information

Part Number	Temp Range	Pin Package	Top Mark	MOQ
YHM2712AW6T	-40°C to 85°C	6 WLCSP	YW LA	3000

T = Tape and reel.
YW: Date Code. Y = year, W = week.
L: The last number of LOTID.
A: YHM2712A

Email Requests to: *SALES@YHMICROS.COM*
YHMicros Website: *WWW.YHMICROS.COM*